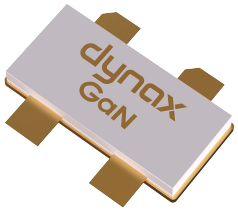
DXG1CH25P-320EF

RF Power GaN Transistor



1. Product profile

1.1 General description

DXG1CH25P-320EF is a 320 W RF GaN HEMT Transistor with first generation RF GaN technology from Dynax, which is ideal for industrial, scientific and medical applications at frequencies from 2400 MHz to 2500 MHz.

Table 1. Typical performance [1]

Freq (MHz)	P_{sat} (dBm)	η_D [2] (%)	G_P [2] (dB)
2435	55.3	73.6	14.6
2450	55.1	73.5	14.0
2465	54.9	73.1	13.1

[1] Typical performance in Dynax Demo with the device soldered onto the heatsink, test condition: V_{DS} = 50 V, V_{GS} = -4.8 V; Input signal CW.

[2] Measured at P_{out} =54.8 dBm.

1.2 Features and benefits

- High Efficiency
- Internally matched for ease of use
- Low thermal resistance providing excellent thermal stability
- Excellent ruggedness
- Excellent reliability

1.3 Applications

- Industry heating
- Welding and heat sealing
- Plasma generation
- Lighting
- Scientific instrumentation
- Medical: Microwave ablation and Diathermy

1.4 Lead-free and RoHS compliant

2. Pinning information

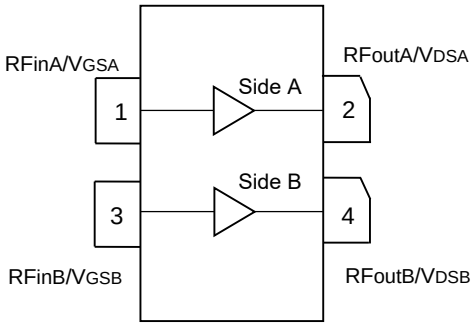


Fig 1. Pin configuration (Top view)

3. Ordering information

Table 2. Ordering information

Part number	Marking	Package type	Packaging information
DXG1CH25P-320EF	DXG1CH25P-320EF	780P2GB	Tray: Suffix = 20 units
			Tape and Reel: Suffix = 100 units; 44 mm Tape width; 13-inch Reel

4. Maximum ratings

Table 3. Maximum ratings

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	150	V
Gate-Source Voltage	V_{GS}	-10 ~ +2	V
Operating Voltage	V_{DS}	0 ~ +55	V
Maximum Forward Gate Current	I_{GMAX}	53.3	mA
Storage Temperature Range	T_{STG}	- 65 ~ +150	℃
Operating Junction Temperature	T_J	225	℃
Absolute Maximum Channel Temperature [1]	T_{MAX}	275	℃

[1] Functional operation above 225℃ has not been characterized and is not implied. Operation at T_{MAX} (275℃) reduces median time to failure by an order of magnitude; Operation beyond T_{MAX} could cause permanent damage.

5. Thermal characteristics

Table 4. Thermal characteristics

Parameter	Symbol	Value	Unit
Side A			
Thermal Resistance at Average Power by Infrared Measurement, Active Die Surface-to-Case $T_{base\text{-}plate}$ = 85 °C, P_D = 57.2 W	R_{thjc}(IR)	1.0	°C/W
Thermal Resistance at Average Power by Finite Element Analysis, Junction-to-Case $T_{base\text{-}plate}$ = 85 °C, P_D = 57.2 W	R_{thjc}(FEA)	1.3	°C/W
Side B			
Thermal Resistance at Average Power by Infrared Measurement, Active Die Surface-to-Case $T_{base\text{-}plate}$ = 85 °C, P_D = 57.2 W	R_{thjc}(IR)	1.0	°C/W
Thermal Resistance at Average Power by Finite Element Analysis, Junction-to-Case $T_{base\text{-}plate}$ = 85 °C, P_D = 57.2 W	R_{thjc}(FEA)	1.3	°C/W

6. ESD protection characteristics

Table 5. ESD protection characteristics

Test methodology	Class
Human Body Model (per JS-001-2012)	1B (> 500 V)
Charged Device Model (per JESD22-C101F)	C3 (> 1000 V)

7. Moisture sensitivity level

Table 6. Moisture sensitivity level

Test methodology	Class
Moisture Sensitivity Level (per J-STD-020)	Level 1

8. Electrical characteristics (TA = 25℃ unless otherwise noted)

Table 7. DC characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Side A					
Drain-Source Leakage Current (V_{GS} = -10 V, V_{DS} = 150 V)	I_{DSS}	-	-	26.6	mA
Drain-Source Breakdown Voltage (V_{GS} = -10 V, I_D = 26.6 mA)	$V_{(BR)DSS}$	150	-	-	V
Gate Threshold Voltage (V_{DS} = 48 V, I_D = 26.6 mA)	$V_{GS(th)}$	-4.0	-2.9	-1.0	V
Gate Quiescent Voltage (V_{DS} = 48 V, I_D = 500 mA)	$V_{GS(Q)}$	-	-2.7	-	V
Side B					
Drain-Source Leakage Current (V_{GS} = -10 V, V_{DS} = 150 V)	I_{DSS}	-	-	26.6	mA
Drain-Source Breakdown Voltage (V_{GS} = -10 V, I_D = 26.6 mA)	$V_{(BR)DSS}$	150	-	-	V
Gate Threshold Voltage (V_{DS} = 48 V, I_D = 26.6 mA)	$V_{GS(th)}$	-4.0	-2.9	-1.0	V
Gate Quiescent Voltage (V_{DS} = 48 V, I_D = 500 mA)	$V_{GS(Q)}$	-	-2.7	-	V

Table 8. RF characteristics (Typical performance – 2450 MHz) [1]

Parameter	Symbol	Min.	Typ.	Max.	Unit
Peak Output Power	P_{sat}	54.4	55.3	-	dBm
Drain Efficiency[2]	η_D	64.0	72.0	-	%
Power Gain [2]	G_P	14.5	16.1	17.7	dB

[1] Typical performance in Dynax DXG1CH25P-320EF production test fixture, test condition: V_{DS} = 50 V, V_{GS} = V_{th}-$V_{goffset}$, $V_{goffset}$=1.6 V, Input signal Pulsed CW, Pulse width = 100 μs, Duty cycle = 10 %.

[2] Measured at P_{out} = 54.4 dBm.

Table 9. Load mismatch

Parameter	Result
VSWR 10:1 at V_{DS} = 50 V, 300 W Pulsed CW output power, Pulse width = 100 μs, Duty cycle = 10%.	No device damage

9. Test information

9.1 Typical application circuit

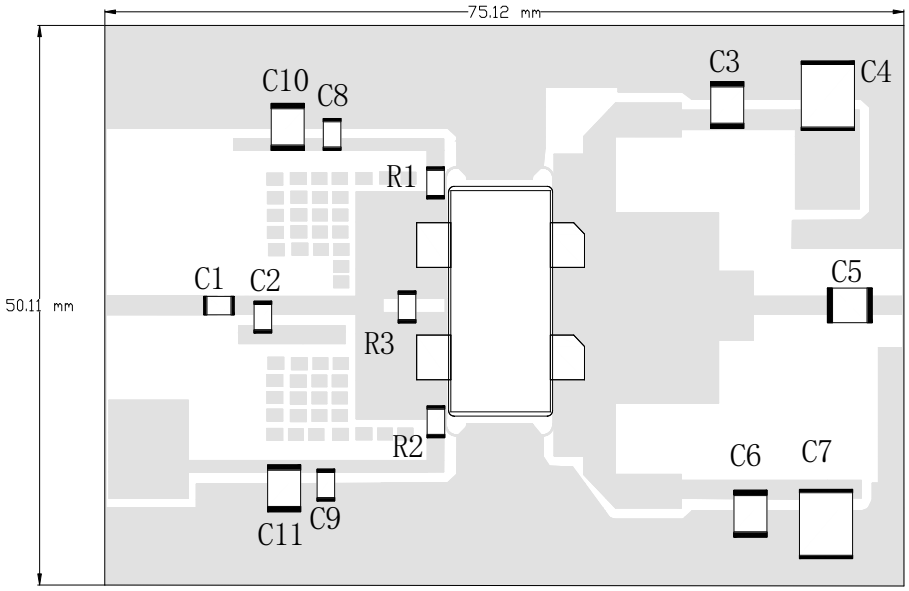


Fig 2. Component layout

Table 10. List of components

S/N	Type	Designator	Description	Value	Vendor
1	Res	R1,R2,R3	RC0805FR_0710RL	10 Ω	Yageo
2	Cap	C1,C8,C9	ATC600F100FW250XT	10 pF	ATC
3	Cap	C2	ATC600F1R3AW250XT	1.3 pF	ATC
4	Cap	C3,C6	ATC100B100JTDC7	10 pF	ATC
5	Cap	C5	ATC800R270J500T	27 pF	ATC
6	Cap	C10,C11	GRM31CZ72A475KE11L	4.7 uF	Murata
7	Cap	C4,C7	C5750X7S2A106KT	10 uF	TDK
8	Transistor	U1	DXG1CH25P-320EF	/	Dynax
9	PCB	/	TC-350 Plus	30 mil	Rogers

9.2 Graphic Data

9.2.1 Pulsed CW

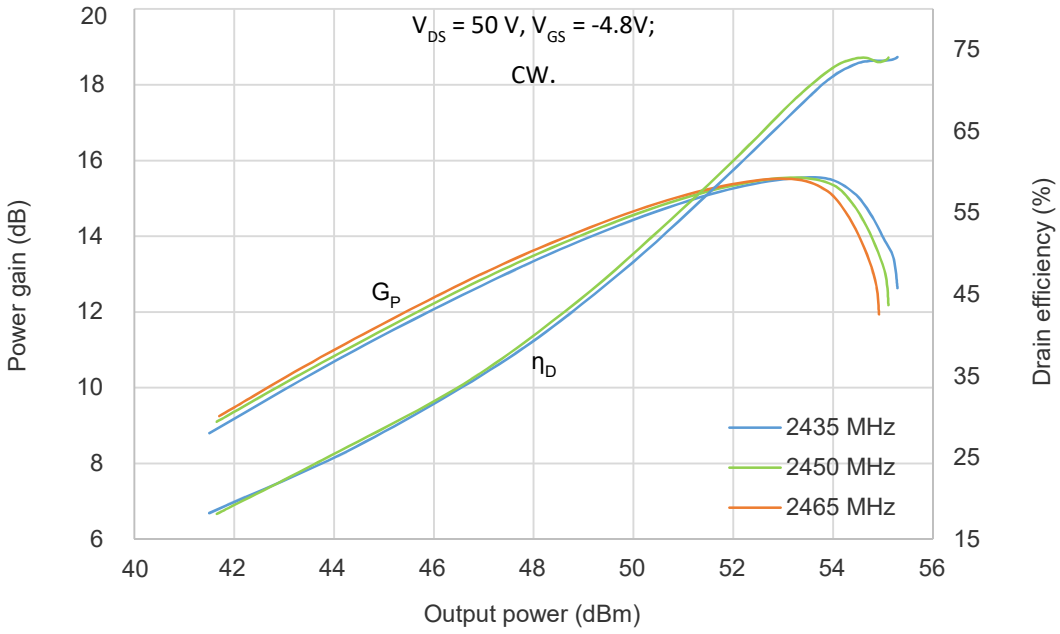


Fig 3. Power gain，Drain efficiency vs. Pulse output power

10. Impedance information

Table 11. Typical impedance of side A [1]

Maximum Output Power						
Freq (MHz)	Z_S (Ω)	Z_L (Ω)	G_P (dB)	P_{sat} (dBm)	P_{sat} (W)	η_D (%)
2400	10.2 - j13.6	3.6 - j4.8	19.0	54.1	257	67.5
2500	9.0 - j8.7	3.8 - j5.3	19.2	54.0	251	67.0
Maximum Drain Efficiency						
Freq (MHz)	Z_S (Ω)	Z_L (Ω)	G_P (dB)	P_{sat} (dBm)	P_{sat} (W)	η_D (%)
2400	10.2 - j13.6	2.1 - j2.1	20.8	52.0	158	80.0
2500	9.0 - j8.7	2.1 - j2.8	20.8	51.9	155	79.3

Table 12. Typical impedance of side B [1]

Maximum Output Power						
Freq (MHz)	Z_S (Ω)	Z_L (Ω)	G_P (dB)	P_{sat} (dBm)	P_{sat} (W)	η_D (%)
2400	10.2 - j13.6	3.6 - j4.8	19.0	54.1	257	67.5
2500	9.0 - j8.7	3.8 - j5.3	19.2	54.0	251	67.0
Maximum Drain Efficiency						
Freq (MHz)	Z_S (Ω)	Z_L (Ω)	G_P (dB)	P_{sat} (dBm)	P_{sat} (W)	η_D (%)
2400	10.2 - j13.6	2.1 - j2.1	20.8	52.0	158	80.0
2500	9.0 - j8.7	2.1 - j2.8	20.8	51.9	155	79.3

[1] V_{DS} = 48 V, I_{DQA} = 500 mA, Pulsed CW, Pulse width = 100 µs, Duty cycle = 10 %.

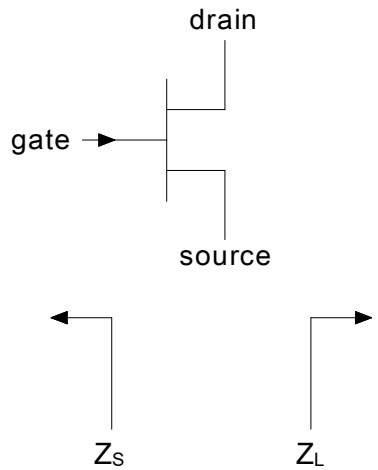


Fig 4. Definition of transistor impedance

11. Median lifetime

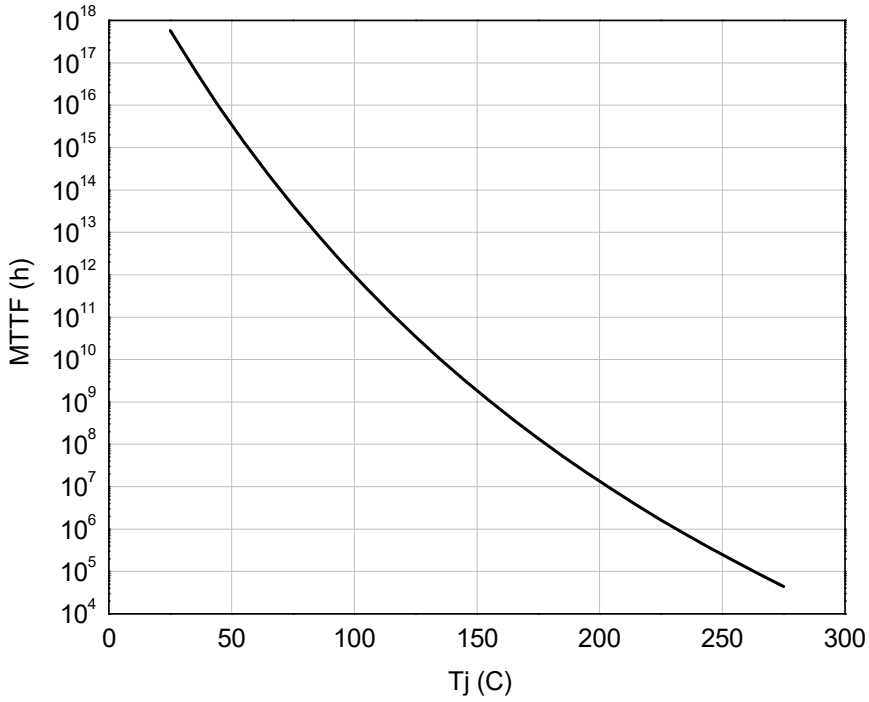
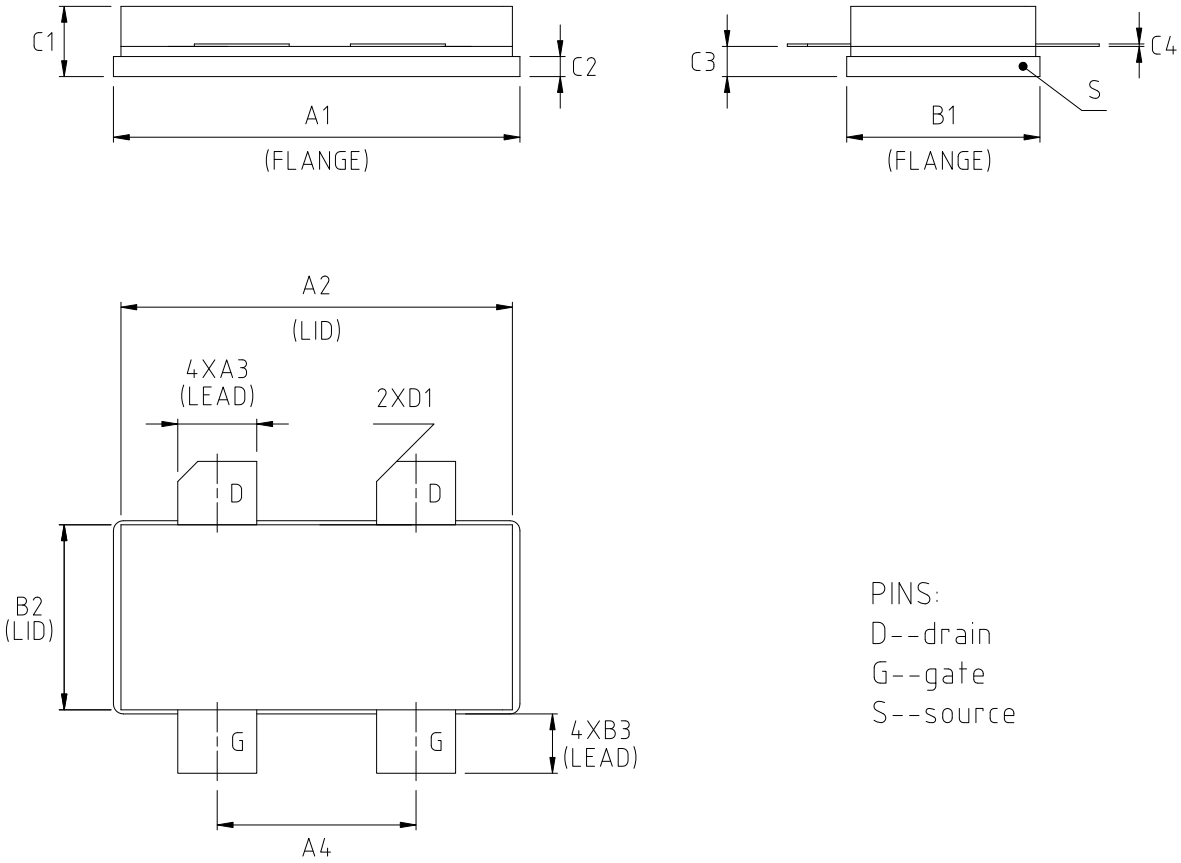


Fig 5. Median lifetime vs. channel temperature

12. Package outline



DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX
A1	0.805	0.815	20.45	20.70
A2	0.772	0.788	19.61	20.02
A3	0.153	0.162	3.87	4.13
A4	0.385	0.395	9.77	10.03
B1	0.380	0.390	9.65	9.91
B2	0.365	0.375	9.27	9.53
B3	0.108	0.128	2.75	3.25
C1	0.130	0.170	3.30	4.32
C2	0.035	0.045	0.89	1.14
C3	0.057	0.067	1.45	1.70
C4	0.003	0.006	0.08	0.15
D1	0.040 45° REF		1.02 45° REF	

Fig 6. Package outline —— 780P2GB

13. Abbreviations

Table 13. Abbreviations

Acronym	Description
CW	Continuous Waveform
ESD	Electro-Static Discharge
GaN	Gallium Nitride
HEMT	High Electron Mobility Transistor
MTTF	Median Time To Failure
VSWR	Voltage Standing Wave Ratio

14. Legal information

14.1 Datasheet status

Document status	Product status	Definition
Objective [short] datasheet	Engineering sample	This document contains data from the objective specification for product development.
Preliminary [short] datasheet	Engineering sample	This document contains data from the preliminary specification.
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